electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts.

2. An apparatus as recited in claim 1 wherein the substrate has a first side and a second side, the plurality of memory devices being disposed on both sides of the substrate.

3. An apparatus as recited in claim 1 wherein the substrate has a first side and a second side, the plurality of channels extending across both sides of the substrate.

4. An apparatus as recited in claim 1 wherein each channel includes a plurality of conductors, the plurality of conductors following a substantially linear path across the substrate.

5. An apparatus as recited in claim 1 wherein each channel includes a plurality of conductors, the plurality of conductors having lengths that are approximately equal.

6. **(Amended)** An apparatus as recited in claim 1 wherein the substrate has one or more surfaces and the memory devices are mounted on such one or more surfaces of the substrate.

7. **(Amended)** An apparatus comprising:

a first substrate having a plurality of memory devices disposed thereon and a first channel portion extending across the first substrate, the first substrate having opposite ends and contacts at the opposite ends to allow communications through the first channel portion via the contacts at the opposite ends of the first substrate;

a second substrate having a plurality of memory devices disposed thereon and a second channel portion extending across the second substrate, the second substrate having opposite ends and contacts at the opposite ends to allow communications through the second channel portion via the contacts at the opposite ends of the second substrate; and

a first connector configured to communicatively couple the first channel portion to the second channel portion through at least some of the contacts of the first and second substrates, wherein the first connector engages contacts at a first of the ends of the first substrate and engages contacts at a first of the ends of the second substrate;

8. An apparatus as recited in claim 7 wherein the coupling of the first channel portion to the second channel portion through the connector forms a channel.

11. An apparatus as recited in claim 7 wherein the first channel portion includes a plurality of conductors following a substantially linear path across the first substrate.

12. An apparatus as recited in claim 7 wherein the second channel portion includes a plurality of conductors following a substantially linear path across the second substrate.

13. An apparatus as recited in claim 7 wherein the first channel portion includes a plurality of conductors having lengths that are approximately equal.

14. An apparatus as recited in claim 7 wherein the second channel portion includes a plurality of conductors having lengths that are approximately equal.

15. An apparatus as recited in claim 7 further including a third substrate coupled to the first connector.

16. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate.

17. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third channel portion including a plurality of conductors following a substantially linear path across the third substrate.

18. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third

channel portion including a plurality of conductors having lengths that are approximately equal.

19. **(Amended)** An apparatus as recited in claim 7 further including a second connector that engages contacts at a second of the ends of the first substrate and engages contacts at a second of the ends of the second substrate.

20. An apparatus as recited in claim 19 wherein the second connector is coupled to a motherboard.

21. **(Amended)** An apparatus comprising:

a motherboard; and

a first memory module having contacts at opposite ends thereof, a first channel portion extending across the first memory module between the contacts;

a second memory module having contacts at opposite ends thereof, a second channel portion extending across the second memory module between the contacts;

a first connector coupling the first memory module to the second memory module through contacts at first ends of the first and second memory modules; and

a second connector that engages contacts at the second ends of the first and second memory modules.

23. An apparatus as recited in claim 21 wherein a channel extends across the first memory module, the second memory module, and the first connector.

24. **(Amended)** A method comprising:

arranging channel portions on a substrate such that the channel portions extend between opposite edges of the substrate;

arranging contacts at the opposite edges of the substrate to allow communication through the channel portions;

arranging channel portion conductors such that the length of the channel portion conductors between opposite edges of the substrate is approximately equal; and

coupling together a pair of such substrates using a connector, a channel extending across the pair of substrates and the connector.

25. A method as recited in claim 24 further including propagating signals through the channel.

26. A method as recited in claim 24 further including arranging a plurality of memory devices on the substrate such that each memory device is coupled to a channel portion.

27. A method as recited in claim 26 further including propagating signals through the channel portions to perform memory operations.

28. A method as recited in claim 24 wherein each channel portion includes a plurality of conductors, each of the conductors having approximately equal lengths along the entire length of the channel portion.

29. A method as recited in claim 24 wherein each channel portion includes a plurality of conductors following a substantially linear path across the substrate.

30. A method as recited in claim 24 wherein channel portions are arranged on both sides of the substrate.

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31. **(New)** A memory system comprising:

first and second memory modules;

each of the first and second memory modules having contacts at first and second opposite ends thereof and having one or more communication channel portions extending between the contacts;

each of the first and second memory modules having a surface and one or more memory devices mounted to the surface, the one or more memory devices being communicatively coupled to the one or more communication channel portions;

one or more board connectors that engage the contacts at the first ends of the first and second memory modules to allow communications through the one or more communication channel portions of the memory modules;

a coupling that engages the contacts at the second ends of the first and second memory modules, the coupling being configured to communicatively couple the one or more channel portions of the first and second memory modules and to thereby form one or more communication channels that each comprise at

least one of the communication channel portions of the first memory module and at least one of the communication channel portions of the second memory module.

32. **(New)** A memory system as recited in claim 31, wherein the communication channel portions comprises a plurality of conductors following substantially linear paths across the respective memory modules.

33. **(New)** A memory system as recited in claim 31, wherein each communication channel portion comprises a plurality of conductors having lengths that are approximately equal.

34. **(New)** A memory module comprising:

a substrate having opposite ends and at least one surface;

contacts at the opposite ends of the substrate;

one or more memory devices mounted to the surface of the substrate; and

one or more communication channel portions extending across the module between the contacts, the one or more communication channel portions being configured to allow communications through the contacts with the one or more memory devices.

35. **(New)** A memory module as recited in claim 34, wherein the substrate has opposing surfaces, and the one or more memory devices comprise at least one memory device mounted on each of the opposing surfaces of the substrate.

36. **(New)** A memory module as recited in claim 34, wherein the substrate has opposing surfaces, and the one or more communication channel portions comprise at least one communication channel portion extending across each of the opposing surfaces of the substrate.

37. **(New)** A memory module as recited in claim 34, wherein each communication channel portion comprises a plurality of conductors that follow a substantially linear path across the substrate.

38. **(New)** A memory module as recited in claim 34, wherein each communication channel portion comprises a plurality of conductors having lengths that are approximately equal.